Performance Analysis of Power Factor Correction for PWM Control based Bridgeless Cuk Rectifier with Positive Output Voltage

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Abstract – This paper presents a single-phase, bridgeless Cuk AC/DC power factor correction (PFC) rectifier with positive output voltage. The rectifier is designed to convert high input voltage to low output voltage which is used for low output voltage product applications. There is the input conduction losses are decreased due to no bridge-diodes required, so the proposed rectifier efficiency can be improved. The proposed rectifier does not need the current loop circuit it needs discontinuous conduction mode (DCM) only. Also, only a single switch is used in the rectifier to simplify the control circuit design. A simple translation method to have the positive output voltage in the Cuk converter is presented in the rectifier to reduce the component counts and the cost as well. The operational principles, steady-state analysis, and design procedure of the proposed rectifier are addressed in detail in this paper. Simulation and experimental results are obtained which verified the validity of the proposed rectifier.

Index Terms – Power factor correction (PFC), Discontinuous conduction mode (DCM), bridgeless, Cuk, positive output voltage.

1. INTRODUCTION

In recent years, switched-mode power supply technologies have developed rapidly. Most switched mode power supplies for electronic products are used to convert AC to DC sources in different applications. The use of a transformer, a bridge rectifier, and capacitors can achieve a DC-output voltage easily, but the input current may be seriously distorted. Therefore, the PFC converters are critically required for AC-DC conversion [1-2]. A variety of circuit topologies have been developed for the PFC applications. The conventional PFC converter is a full bridge rectifier followed by a boost converter, as shown in Fig. 1. The converter is widely used, because of its simplicity. However, due to boosting behavior of the converter, the output voltage is always greater than the input voltage. In many applications, such as low voltage and low-power supplies, it is desired to have the output voltage lower than the peak of input voltage. A buck-type converter is thus required. The buck converter is seldom used in the PFC application, since as the input current of the buck converter is discontinuous, it would lose control when the input line-voltage is lower than the output voltage. The renewable energy is used to track maximum power point and multilevel inverters are used to convert DC-AC for various applications [3-9]. Also, to filter the input current, additional passive filter must be used at the buck converter input. Many algorithms are used to give gate generations [10-13].

Besides, the buck PFC converter may lead to increased total harmonic distortion (THD) and reduced power factor (PF) [14]. Therefore, in such applications, converters like buck-boost, single ended primary inductor converter (SEPIC) or Cuk converter are often used next to a full-bridge rectifier, as shown in Fig. 2 to Fig. 4 [15-23], to have a PFC converter with low output voltage.

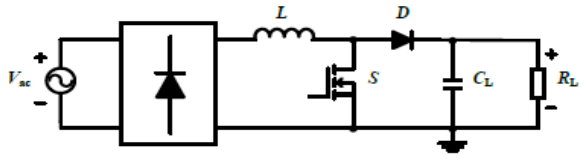

Fig. 1 Conventional boost PFC converter

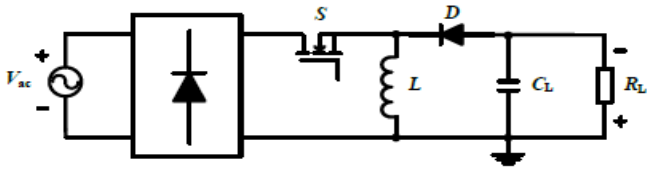

Fig. 2 Conventional buck-boost PFC converter

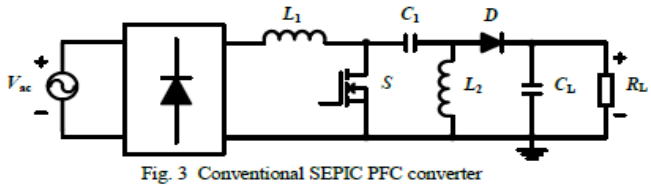

Fig. 3 Conventional SEPIC PFC converter

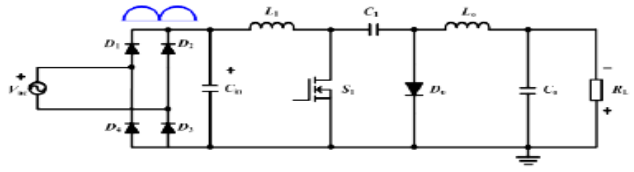

Fig. 4 Conventional Cuk PFC converter

All the converters mentioned above can be used in DCM or continuous conduction mode (CCM). While operating in DCM to shape the input current sinusoidally, these converters have intrinsic PFC characteristics at fixed duty ratio [14], there is no need of any control circuit. However, the drawbacks of buck-boost converter operating in DCM are high-current stress on semiconductor devices and discontinuous input current, which increases the THD.

On the other side, SEPIC and Cuk converters are the ones whose input currents are continuous, while operating in DCM with the output voltage lower than the input voltage. Similar to the boost converter, SEPIC converter has the disadvantage of discontinuous output current, resulting in relatively high output ripple.

The Cuk converter offers several advantages in PFC applications, such as easy implementation of transformer isolation, natural protection against inrush current occurring at start-up or overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the DCM topologies.

Unlike the SEPIC converter, the Cuk converter has both continuous input and output currents with a low current ripple. Thus, for applications requiring low-current ripples at the both input and output ports of the converter, the Cuk converter seems to be a better candidate in the basic converter topologies.

In practical applications the DCM operation of the Cuk converter significantly increases the conduction losses, due to the increased current stress on the circuit components. However, using CCM for low-power applications, it requires extra components to achieve PFC performance. As a result, additional circuit cost is increased. This limits the DCM operation of the Cuk converter only in low-power applications (< 300 W).

In a conventional PFC Cuk rectifier as shown in Fig. 4, the current flows through bridge diodes and the power switch *(S1)* during the switch ON-time, and through bridge diodes and the output diode *(Do)* during the switch OFF-time. Thus, during each switching cycle, the current flows through three power semiconductor devices. As a result, the significant conduction loss caused by the forward voltage drop across the bridge diodes degrades the converter's efficiency, especially at low line-input voltage. To reduce the conduction losses, the number of semiconductor devices should be reduced in the current path. Some methods to reduce conduction losses in Cuk and SEPIC converters are proposed.

The control circuits are complex using two main switches in the Cuk PFC topology. The bridgeless SEPIC converter introduced in [18] consists of two SEPIC converters, each of which is used for a half-line cycle. Thus, the number of devices and the cost are increased. As mentioned above, the SEPIC converter has the disadvantage of discontinuous output current, resulting in a relatively high output ripple.

The Cuk and SEPIC converters have negative output voltages. Therefore, the extra requirement is an inverse amplifier circuit to translate the negative into the positive voltage. The additional inverse amplifier circuit thus increases the cost.

2. PROPOSED BRIDGELESS CUK PFC RECTIFIER WITH POSITIVE OUTPUT VOLTAGE

Fig. 5 shows the proposed initial bridgeless Cuk PFC rectifier, which has a negative output voltage, like the existing Cuk PFC rectifier. As noted, for this circuit an inverting circuit to transfer the negative to the positive output voltage is still required for analog feedback control, as shown in Fig. 6.

To obtain the positive output voltage without the inverting amplifier circuit, we transfer the polarity of all the components in Fig. 5 into those as shown in Fig. 7, and obtain the proposed bridgeless Cuk PFC rectifier in Fig. 8. Thus, the feedback control circuit is simpler and the cost can also be reduced, as compared with the conventional feedback control circuit as shown in Fig. 6, though the power switch employed in the proposed circuit is floated with a high-side gate driver needed.

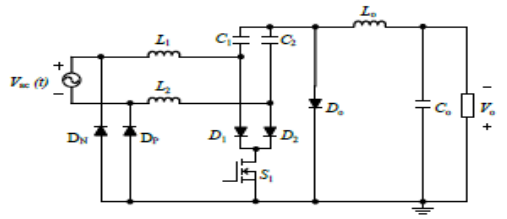

Fig. 5 Proposed Bridgeless Cuk power factor correction rectifier with negative output voltage

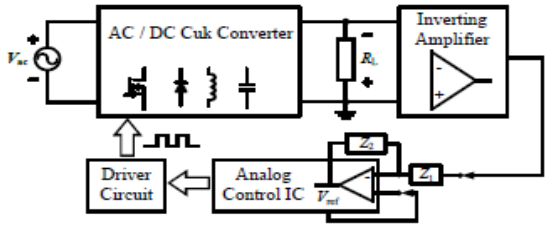

Fig. 6 Blocking Diagram of the conventional Cuk PFC circuit (with negative output voltage)

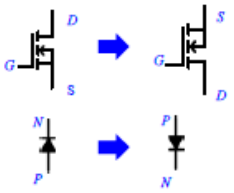

Fig. 7 Transferring the polarity of all components in the proposed initial topology in Fig. 5

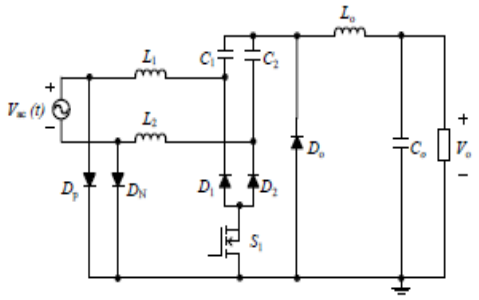

Fig. 8 Proposed Bridgeless Cuk PFC rectifier with positive output voltage

Before analyzing the proposed rectifier, the analysis of the circuit supposes that the converter is operating at steady state with the following assumptions:

1.The ON-state resistance RDS_ON and parasitic capacitances of the main switch S1 and the forward voltage drops (Vd) of the diodes are neglected.

2.The input capacitances are large enough such that during a switching period (Ts) their voltages are considered to be constant.

3.The output capacitor Co is sufficiently large that the output voltage is considered to be constant.

4.The proposed converter is operated in the DCM.

5.Due to symmetry of the circuit, it is sufficient to analyze the circuit during the positive half-cycle of the input voltage.

A. Principles of Operation

Mode I [t0 - t1]: This mode starts when switch S1 is turned ON, as shown in Fig. 9 and Fig. 10. Input inductors L2 starts to charge linearly in slope of Vac(t)/L2, and diode Dp is forward biased by the indictor current iL2. The voltage across Lo is equal to Vac(t), thus iLo increases linearly in slope of Vac(t)/Lo. The inductor currents of L2 and Lo during this mode are given by

$$Di_{Ln}/dt=v_{ac}(t)/_{Ln},n=2,0 \quad (1)$$

Accordingly, the peak current through the active switch S1 is given by

$$Is1,_{pk=(Vm/Lo)}D_1T_s \quad (2)$$

whereVm is the amplitude of the input voltage Vac(t), D1 is the switch duty cycle, and Le is the parallel combination of inductors of L1, L2, and Lo.

Mode II [t1 - t2]: This mode starts when switch S1 is turned OFF and diode Do is turned ON, simultaneously, as shown in Fig. 11 and Fig. 12. Input inductor L2 starts to discharge linearly in slope of Vac(t)/L2, and diode Dp is forward biased by the indictor current iL2. The voltage across Lo is equal to Vo, thus iLo decreases linearly in slope of Vo/Lo. Note that diode Do is turned OFF at zero current. The inductor currents of L2 and Lo during this mode are given by

$$Di_{L2}/dt=(-V_{ac}(t)/L2) \quad (3)$$

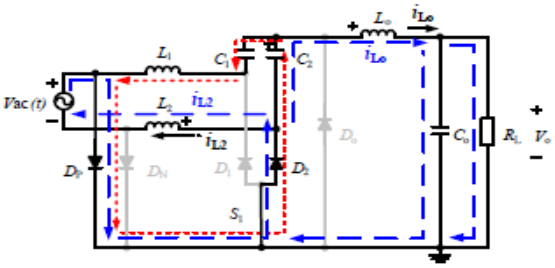

Fig. 9 The equivalent circuit in mode I (Switch S_1 is turned ON)

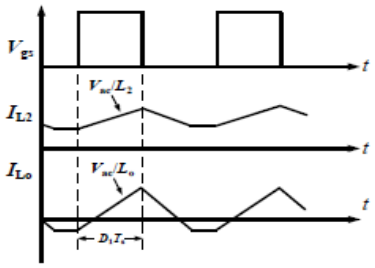

Fig. 10 Theoretical DCM waveforms during one switching period T_s in mode I (Switch S_1 is turned ON)

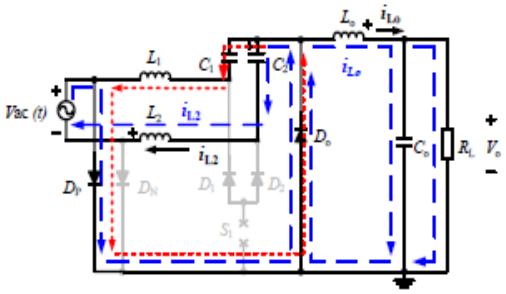

Fig. 11 The equivalent circuit in mode II (Switch S_1 is turned OFF)

Fig.12

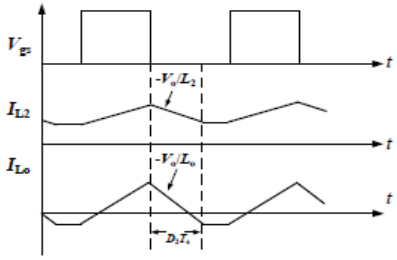

Fig. 12 Theoretical DCM waveforms during one switching period T_s in mode II (Switch S_1 is turned OFF)

$$Di_{Lo}/dt=(-Vo/L0) \quad (4)$$

Mode III [t2 - t3]: During this interval, only diode *D*p conducts to provide a path for *i*L2, as shown in Fig. 13. Accordingly, the inductors *L*2 and *L*o in this interval behave as constant current source. Thus, the voltage of inductors (*L*2 and *L*o) is zero. Capacitor *C*2 is being charged by the inductor current *i*L2 and the energy of capacitor *C*o is released to load.

This is a freewheeling mode. The theoretical waveforms in this mode are shown in Fig. 14. This mode lasts until the start of a new switching period. The turn-OFF time of the switch and the output diode is given by

$$t_{off} = T_s - t_{on} - t_{don} \quad (5)$$

where*t*on is the conducting interval of switch *S*1 and *t*don is that of the output diode *D*o.

According to Equations (2) and (4), the normalized length of Mode II period can be obtained as follows:

$$D_2 = D1/m \sin\omega t \quad (6)$$

where*ω* is the line angular frequency, and *M* is the voltage conversion ratio (*M*= *V*o/*V*m).

B. Analysis and Design of the Proposed Cuk PFC Rectifier

(1) Design of Input Inductors

According to the relationship of input current ripple (Δ*I*L2), as shown in Fig. 10, and input voltage (*V*ac) in positive-half cycle, the values of input indictor (*L*1 and *L*2) can be obtained below:

$$L2 = Vac(t)D1/\Delta I_{L2} f_s \quad (7)$$

(2) Voltage Conversion Ratio M

The voltage conversion ratio M in terms of the rectifier parameters can be obtained by applying the power-balance principle below,

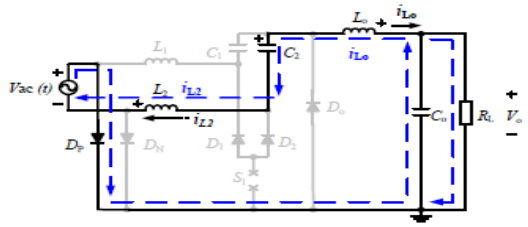

Fig. 13 The equivalent circuit in mode III (Switch S_1 is turned OFF)

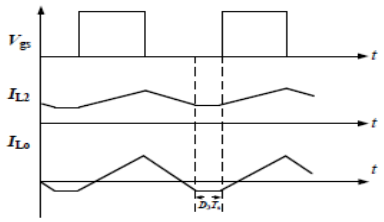

Fig. 14 Theoretical DCM waveforms during one switching period T_s in mode III (Switch S_1 is turned OFF)

$$P_{in}(t) = 2/T \int V_{in}(t)\, I_{in}(t)\, dt \quad (8)$$

According to the large-signal model of the DCM switch network, as shown in Fig. 15, it is noted that the average input current can be given as follows:

$$I_{in}(t) = V_{in}(t)/R_{in} \quad (9)$$

Where *Rin* is defined as the input resistance and given by

$$R_{in} = 2L_e/D_1^2\, T_5 \quad (10)$$

Evaluating (8) by using (9) and applying the power balance between the input and output ports, the voltage conversion ratio can be given by

$$M = V_o/V_m \quad (11)$$

(3) Boundaries between CCM and DCM

To operate in DCM, the following inequality must be satisfied:

$$D_2 = <1-D1 \quad (12)$$

Substituting Equation (6) into (12) and applying (10) and (11), the following condition for DCM is obtained:

$$K_e \le K_{e\,cri} = 1/2(M+\sin(\omega t))^2 \quad (13)$$

where the parameter *K*e is expressed as follows:

$$K_e = 2L_e/R_l T_s \quad (14)$$

It is obvious that from Equation (13) the value of *K*e_crit depends on the line angle *ωt*. Thus, the minimum and maximum parameters of *K*e_crit can be obtained, respectively:

$$K_{e\text{- }cri(min)} = 1/2(M+1)^2 \quad (15)$$

$$K_{e\text{- }cri(min)} = 1/2M^2 \quad (16)$$

Therefore, for *K*e<*K*e_crit(min), the proposed bridgeless Cuk PFC rectifier with positive output voltage always operates in DCM.

(4) Selection of Input Capacitors

In the Cuk converter as PFC, voltages of the input capacitors *C*1 and *C*2 should be nearly constant value within the switching period *T*s and follow the input voltage profile within a line period *TL*. Also, the input capacitors *C*1 and *C*2 should not cause low-frequency oscillations with the converter inductors. Thus, the energy transfer capacitors *C*1 and *C*2 are determined based on inductor *L*1, *L*2 and *Lo* values such that the line frequency (*fL*) should be well below the switching frequency (*fs*). And a better initial approximation for choosing the resonant frequency (*fr*) is given by (17) and (18).

$$f_l < f_r < f_s \quad (17)$$

$$f_r = 1/2\pi(c_1(L_1+L_0)) \quad (18)$$

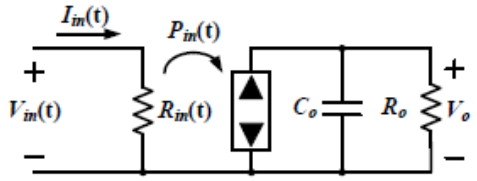

Fig. 15 Large signal model [18] of the proposed Cuk PFC rectifier

(5) Design of Output Capacitor Co

Output ripple frequency of the converter is two times of the input frequency. In the worst case, the output current during the half period of ripple frequency is provided by the output capacitor. Therefore, *Co* can be obtained as follows:

$$C_o=P_0/4f_lV_0\Delta V_0 \quad (19)$$

(6) Stresses on Semiconductor Devices

According to Fig. 11, we may derive the following expressions about the stresses on semiconductor devices as functions of input/output voltages and currents on inductors.

$$V_{D,max}=V_{sw,max}=V_{ac,max}+V_0 \quad (20)$$

where *VD*,max and *ID*,max are the maximum voltage and current stresses on diodes *Dp*, *Ds*, *D*1, *D*2 and *Do*; *Vsw*,max and *Isw*,max are the maximum voltage and current stresses on switches *S*1, respectively; *Vac*,max and *Iac*,max are the maximum input voltage and current; Δ*IL* is the current ripple of *L*1 or *L*2, and *IL*2,min is the minimum current of *L*2.

3. EXPERIMENTAL RESULTS

By following the specification given in Table I and the design procedure described above, components and parameters used in the proposed power-stage circuit are listed in Table II for verification of the proposed rectifier.

The experimental results show that *S*1 turns on under ZCS condition and *D*o turns off under ZCS condition, as shown in Fig. 14 to Fig. 16, respectively. Therefore, reverse recovery problem of the main diode is resolved by employing the proposed Cuk rectifier in DCM.

The experimental results of the input voltage and current waveforms are shown in Fig. 11 to Fig. 15 for 20%, 50%, 80% and full (150W) loads, respectively. Fig. 18 shows the experimental waveforms of capacitors *C*1 and *C*2 at full load.

As shown in Fig. 10 for the measured current harmonics, it can be observed that the IEC 61000-3-2 Class D limits of the current harmonics are well met by the proposed Cuk rectifier. The experimental results of the PF and the THD values of the input current for different loads of 20% to full loads (*V*in=110Vrms). The PF is about 0.9961 and the THD in percentage of the input line current is 2.66% for the full power output of 150 W.

Since the proposed rectifier has the functions of ZCS turn On and ZCS turn-off (for the output diode), the switch and output diode losses can be significantly decreased at full load. The measured efficiency from 20% to full loads of the prototype rectifier at line voltages of 90 Vrms, 110 Vrms, and 130 Vrms are shown. It reveals that all the efficiencies of different loads for the line voltage of 110 Vrms are above 91%. The best efficiency 96.2% is obtained at high line-voltage of 130 Vrms at full load, and the worst efficiency 89.7% is observed at low line-voltage (90 Vrms) for 20% load.

TABLE I
SPECIFICATION OF THE PROPOSED RECTIFIER

Specifications	
Input Voltage V_{in}	90-130 V_{rms}
Output Voltage V_{out}	48 V_{dc}
Rated Power P_{out}	150 W
Switching Frequency f_s	100 kHz

TABLE II
COMPONENT PARAMETERS USED IN THE PROPOSED CIRCUIT

Device	Component	Part/Value
Power Switch	Main Switches S_1	IXFH3650P
Diodes	Input Diodes D_p and D_n	MBR20200CT
	Series Diodes D_1 and D_2	STTH6003CW
	Output Diode D_o	
Inductors	Input Inductors L_1 and L_2	1 mH
	Output Inductor L_o	22 uH
Capacitors	Input Capacitors C_1 and C_2	1 uF/400V
	Output Capacitor C_o	2 mF/100V
Control IC	UC 3525 (Voltage mode)	

The comparisons of test conditions and power components are used between the proposed circuit and the one. As shown in the table, the inductor used in the proposed circuit is smaller than the one in under same rated power output.

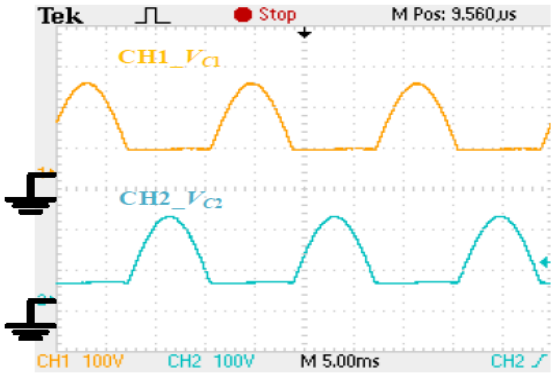

Fig. 16 Experimental waveforms of VC1 and VC2 at full load*S*1 at full load (150 W)

In addition, for the same output voltage of 48 Vdc the efficiency 96.2% of the proposed circuit at full load of 150W

with input voltage of 130 Vrms is compared to 93.2% at full load of 150W with input voltage of 100 Vrms [18] and 93.0% at full load of 100W with input voltage of 220 Vrms. Since the efficiencies available from the experimental results in the literature are for different power output ratings and input voltages of the circuits compared, only the efficiencies at their full loads are compared as above. However, it should be noted that the comparisons are only for references, due to different test conditions and components employed in the circuits.

4. CONCLUSIONS

In this paper, the Cuk PFC rectifier with positive output voltage has been proposed and experimentally verified. The experimental results have shown good agreements with the predicted waveforms analyzed in the paper. The power factor of the circuit has 0.99 above at all the specified input and output conditions. Satisfaction of the IEC 61000-3-2 requirements can be easily achieved by the proposed circuit. Moreover, with higher efficiency and high power factor the proposed topology is able to be applied to most of the consumer electronic products of 150W rating in the market. Also, with only a single switch employed, the implemented system control circuit is simple to achieve high power factor by applying any PWM control IC. Moreover, as required in the traditional Cuk circuit, transferring the original negative output voltage to the positive one is not needed in the proposed Cuk topology. Convenience of using the Cuk rectifier can thus be obtained.

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